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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,032	08/22/2003	Oliver Dieter Landolt	10011475-1	9255

7590 12/14/2005

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EXAMINER	
LUI, DONNA V	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,032	LANDOLT, OLIVER DIETER	
	Examiner	Art Unit	
	Donna V. Lui	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-20* is/are allowed.

6)☒ Claim(s) *1,7 and 8* is/are rejected.

7)☒ Claim(s) *2-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In the detailed description, page 10, line 15, the pull-down transistor was referenced to 126. The reference is incorrect and should be changed to correspond to 128.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1 and 7-8** are rejected under 35 U.S.C. 102(b) as being anticipated by Itakura et al. (Pub No.: 2002/0180685).

With respect to **Claim 1**, Itakura discloses a driving circuit *(See figure 31)*. Itakura teaches the driving circuit to comprise an output transistor *(Mp43)* connected between a voltage terminal *(Vdd)* and an output node *(node that is common to the resistor Rf and the terminals of Mp43 and Mn43)* to produce an output signal on the output node. Itakura teaches the output transistor to include a control terminal *(the control terminal is connected to a node common to Cf1, where the node connects to the terminal of Mp45)*; a current source *(Ib1)* connected to the control terminal of the output transistor to provide a reference current *(the connection of the current source to the control terminal of the*

output transistor is either through Mn41 when the switch SW20 is closed or through Mn42); a feedback capacitor *(Cf1)* connected from the output node to the control terminal of the output transistor to control the output transistor as a function of a difference between current through the capacitor and the reference current.

With respect to **Claim 7**, Itakura teaches a first switch *(See figure 31, Mn41)* located between the voltage terminal and the output transistor *(note that the connection to the output transistor is through the terminal of the output transistor that is common to Cf1 and the output node, designated with a dotted line; the connection to the voltage terminal is through either Mp44 or through both SW20 and Mp45)* and a second switch *(Mn42)* located between the current source and the control terminal of the output transistor *(note that the connection to the control terminal is the connection area that is common to Mp45, Cf1, SW20 and Mp43)*, the first and second switches being controlled by an input signal *(Itakura notes in the specification that IN+ and IN- are representative of input signals; p. 4, [0065], lines 11-12).*

With respect to **Claim 8**, Itakura teaches a second output transistor *(Mn43)* connected between the output node *(node that is common to the resistor Rf and the terminals of Mn43 and Mp43)* and a second voltage terminal *(Vss)*, the second output transistor including a control terminal *(the control terminal is connected to a node common to Cf2, where the node connects to the terminal of Mn45)*; a second current source *(Ib2)* connected to the control terminal of the second output transistor *(the connection of the current source to the control terminal of the output transistor is either*

through Mp41 when the switch SW21 is closed or through Mp42); and a second feedback capacitor *(Cf2)* connected from the output node to the control terminal of the second output transistor.

Allowable Subject Matter

4. **Claims 2-6** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to **Claim 2**, reference Itakura teaches a driving circuit but does not teach the driving circuit to further comprise a memory operatively connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal of the output transistor from a previous operating cycle in which the output transistor was activated.

With respect to **Claim 5**, reference Itakura teaches a driving circuit but does not teach the current source configured to generate a reference current proportional to a reference voltage and a reference frequency.

5. **Claims 9-20** are allowed.

6. The following is an examiner's statement of reasons for allowance:

With respect to **Claim 9**, Itakura does not teach a driver circuit comprising: an output transistor connected between a voltage terminal and an output node to produce an output signal on the output node, the output transistor including a control terminal; a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated; a current source connected to the control terminal of the output transistor to provide a reference current; and a feedback capacitor connected from the output node to the control terminal of the output transistor to control a rate of signal change on the output node.

With respect to **Claim 16**, Itakura does not teach a method for driving an electrical device, where the method comprisses: receiving an input signal; applying a stored signal to an output transistor in response to the input signal to produce an output signal on an output node; and controlling the output signal on the output node using a difference between a reference current and current capacitively fed back from the output node.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DL

Donna V Lui
Examiner
Art Unit 2675

KENT CHANG
PRIMARY EXAMINER